P.R. GOVERNMENT COLLEGE (A), KAKINADA

B.Sc. II Year - Electronics – Semester – 3

PAPER – 3 [Code: EL3202]

w.e.f. 2018-19 ADMITTED BATCH

DIGITAL ELECTRONICS

4 Hours/Week [Total: 60 hrs] **Credits: 3**

Course Learning Outcomes

The subject aims:

- ✓ Knowledge of Number System
- ✓ Comprehension about Logic Gates
- ✓ Know the applications of Semiconductor Memories
- ✓ Evaluate Combinational Circuits
- ✓ Analysis Karnaugh maps

Learning Outcomes:

Students will be able to:

- ➢ Recall Binary number system.
- ➢ Recognize Universal building blocks
- ➢ Observe Flip flops-RS,D flip flops-JK and JK master-slave
- ➢ Demonstrate Logic families

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SYLLABUS

Unit – I (12 hrs)

Number system and codes:

Decimal, Binary, Hexadecimal, Octal, BCD, Conversions – Binary to Decimal vice versa – Binary to Hexa decimal vice versa, Decimal to Hexa decimal vice versa, Complements (1's and 2's,), Addition, Subtraction. Gray code & Excess-3 Code conversion of - BCD to Grey vice versa – BCD to Excess 3 Code vice versa.

Unit- II (12 hrs)

Boolean algebra and theorems:

Boolean algebra, De-Morgan's laws. Logic gates – AND, OR & NOT, NAND, NOR, EX-OR, EX-NOR, realization of basic gates from NAND & NOR. Minimization Techniques (Karnaugh Map Method: 2 & 4 variables), don't care condition. Standard representation of logic functions (SOP and POS),

Unit-III (15 hrs)

Combinational Digital circuits:

Adders-Half & full adder, Parallel binary adder. Subtractor-Half and full subtractors, Multiplexers (2:1, 4:1)) and Demultiplexers (1:2, 1:4), Encoder (8-line-to-3-line) and Decoder (3-line-to-8-line).

UNIT-IV (9 hrs)

IC-Logic families:

TTL logic (NAND gate), DTL logic, RTL Logic, CMOS Logic families (NOR gate).

UNIT-V (12 hrs)

Sequential Digital circuits & Registers:

Flip Flops: S-R FF, J-K FF, T & D type FFs, Master-Slave J-K FFs and their Truth tables, registers: Types – SIPO, SISO, PIPO, and PISO.

TEXT BOOKS:

1. M.Morris Mano, "Digital Design "3rd Edition, PHI, New Delhi.
2. Ronald J. Tocci. "Digital Systems-Principles and Applications" 6/e. PHI. New Delhi. 1999. (UNITS I to IV)
3. G.K.Kharate-Digital electronics-oxford university press
4. S.Salivahana&S.Arivazhagan-Digital circuits and design
5. Fundamentals of Digital Circuits by Anand Kumar

Reference Books:

1. Herbert Taub and Donald Schilling. "Digital Integrated Electronics". McGraw Hill. 1985.
2. S.K. Bose. "Digital Systems". 2/e. New Age International. 1992.
3. D.K. Anvekar and B.S. Sonade. "Electronic Data Converters: Fundamentals & Applications". TMH. 1994.
4. Malvino and Leach. "Digital Principles and Applications". TMG Hill Edition.

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MODEL QUESTION PAPER

Note: - Set the question paper as per the blue print given at the end of this model paper.

Time: $2\frac{1}{2}$ Hrs. Max.Marks: 60

Section	Questions to be given	Questions to be answered	Marks
A	5	3	3 x 10M = 30M
B	9	6	6 x 5 M = 30M
Total	14	9	60M

Blue Print

Chapter Name	Essay Questions 10 marks	Short Questions 5 marks	Problems 5 marks	Marks allotted
1. **Number system and codes**	1		2	20
2. **Boolean algebra and theorems**	1	1	1	20
3. **Combinational Digital circuits**	1	2	---	20
4. **IC-Logic families**	1	1	---	15
5. **Sequential Digital circuits & Registers**	1	2	---	20
Total Marks				95

Note: At least two problems should be answered.

QUESTION BANK

DIGITAL ELECTRONICS
ESSAY QUESTIONS

UNIT-I: - Number system and codes:

1. Explain Decimal, Binary, Hexadecimal Conversions with example
2. Explain Octal, BCD Conversions with example
3. Explain Decimal to Hexa decimal vice versa with example
4. Explain Binary to Hexa decimal vice versa with example
5. Explain Binary to Decimal vice versa with example
6. Explain Gray code & Excess-3 Code conversion with example
7. Explain BCD to Excess 3 Code vice versa with example
8. Explain BCD to Grey vice versa with example

UNIT-II: - Boolean algebra and theorems:

1. Explain Logic gates – AND, OR & NOT, NAND, NOR, EX-OR, EX-NOR
2. Draw and explain realization of basic gates from NAND & NOR.
3. Explain representation of logic functions (SOP) with example.
4. Explain representation of logic functions (POS) with example.

UNIT-III: - Combinational Digital circuits:

1. Draw and explain half adder and full subtractor.
2. Draw and explain Full adder.
3. Design Encoder (8-line-to-3-line)
4. Design Decoder (3-line-to-8-line).

UNIT-IV: - IC-Logic families:

1. Draw and Explain TTL logic (NAND gate)
2. Draw and explain CMOS Logic families (NOR gate).

UNIT-V: - Sequential Digital circuits & Registers:

1. Draw and explain Master-Slave J-K Flip flop
2. Draw and explain S-R Flip Flop, J-K Flip Flop.

SHORT ANSWER TYPE QUESTIONS

UNIT-II: - Boolean algebra and theorems:

1. Explain Minimization Techniques (Karnaugh Map Method: 2 variables)
2. and don't care condition with two examples
3. Explain Minimization Techniques (Karnaugh Map Method: 4 variables) and don't care condition with example

UNIT-III: - Combinational Digital circuits:

1. Design 2:1 Multiplexer, and write a brief explanation of it.
2. Design 4:1 Multiplexer, and write a brief explanation of it.
3. Design 1:4 Demultiplexer, and give explanation of it.
4. Design 1:2 Demultiplexer, and give explanation of it.
5. Draw and explain half subtractor.
6. Draw and explain Parallel binary adder.

UNIT-IV: - IC-Logic families:

1. Draw the DTL logic. explain its operation.
2. Draw and explain RTL Logic.

UNIT-V: - Sequential Digital circuits & Registers:

1. Draw and explain T type Flip Flops?
2. Draw and explain D type Flip Flops?
3. Draw and explain SIPO.
4. Draw and explain SISO.
5. Draw and explain PIPO.
6. Draw and explain PISO.

PROBLEM:

UNIT-I: - Number system and codes:

1. Find 1's complement of $(1\ 1\ 01)_2$ and $(1\ 0\ 1\ 1)_2$
2. Find 1's complement of 10 11 1 0 0 1
3. Find 2's complement of $(1\ 0\ 0\ 1)_2$ $(1\ 1\ 1\ 0)_2$
4. Find 2's complement of $(1\ 0\ 1\ 0\ 0\ 0\ 1\ 1)_2$
5. Subtract 101011_2 from 111001_2 using the 1's complement method.
6. Subtract 111001_2 from 111001_2 using the 1's complement method.
7. Subtract 101011_2 from 111001_2 using the 2's complement method.
8. Subtract 111001_2 from 111001_2 using the 1's complement method.

UNIT-II: - Boolean algebra and theorems:

1. Reduce F (A,B,C,D) = Σ(0,1,2,4,7,10,15) using k-map.
2. Reduce F (A,B,C,D) = π (0,1,3,4,5,7,9,10,11,13,14,15) using k-map.
3. Reduce F (A,B,C,D) = Σ (1,3,5,7,9,11,10,8) using k-map.
4. Reduce F (A,B,C,D) = π (1,3,5,7,9,11,10,8) using k-map.